IN THE DRAWINGS

Figure 7 contains an error, whereby the emitter of transistor (Q33) is missing a connection to the isolation terminal (ISO). The correct connection should show emitter (38) of transistor (Q33) coupled to the isolation region (ISO), as recited at p. 5, lines 16-17 of the specification, "*transistor Q33 with ... emitter connected to the isolation region ISO.*" A corrected Figure 7 is presented herewith for the Examiner's consideration. The correction is shown on the figure in red. Review and approval of the corrected Figure 7 is respectfully requested. No new matter has been added in correcting the figure.

IN THE CLAIMS

Please amend claims 3 and 4, as shown below. No new matter is being added.

Applicant presents the claims as amended below and encloses a separate sheet indicating the amendments to the claims with bracketing and underlining.

3. (Amended) An integrated circuit according to claim 2, wherein said first bipolar transistor is a vertical transistor having an emitter formed by said substrate, a collector formed by a second doped region of the first conductivity type, and a base formed by a first doped region of the second conductivity type formed in the substrate and within the first doped region.

4. (Amended) An integrated circuit according to claim 3, wherein said first and third bipolar transistors are isolated from the substrate by said isolation region.

Please add the following new claims:

7. (New) A semiconductor device, comprising:

(A) a vertical power component having a terminal formed by a substrate of a first conductivity type;

(B) a control circuit, isolated from the substrate by an isolation region of a second conductivity type; and

(C) a protection structure against polarity inversion of a substrate potential, comprising:

(i) a first bipolar transistor having an emitter connected to said isolation region and a collector connected to a reference potential input of the integrated circuit;

(ii) a bias circuit that biases the first bipolar transistor in a reverse saturation mode when the substrate is at a potential higher than a reference potential;

(iii) a second bipolar transistor having an emitter connected to the substrate and a base connected to the isolation region; and

(iv) a high impedance means that couples the isolation region to the substrate when the substrate potential is lower than the reference potential.

8. (New) The device of claim 7, wherein the second bipolar transistor forms a regulation loop that reduces parasitic transistor action from affecting the first bipolar transistor and the bias circuit.

9. (New) The device of claim 7, wherein the vertical power component comprises a vertical power bipolar transistor.

REMARKS

In response to the Office Action mailed August 28, 2001, the applicant respectfully requests reconsideration and submits the following remarks. Claims 3 and 4 have been amended, with no new matter being added thereby. Support for the amendments can be found in the specification, e.g., at p.6, lines 25-30 and at p.5, lines 31-32, as well as in Figure 7. Claims 3 and 4 have been rephrased and/or corrected to more accurately conform to the subject matter, as found in the specification and figures. Claims 7-9 are newly-added, with claims 8 and 9 depending from independent claim 7. No new matter has been added.

Claim Rejections under 35 U.S.C. §112

At paragraph 3 of the Office Action, claims 3-6 were rejected under 35 U.S.C. §112, first paragraph, as containing subject matter which was not described in the specification. The